3-MHz 2A Step Down Converter in 2x2 SON Package

Check for Samples: TPS62065, TPS62067

FEATURES

- **3 MHz Switching Frequency**
- **V_{IN} Range from 2.9V to 6V**
- **Up to 97% Efficiency**
- **Power Save Mode / 3MHz Fixed PWM Mode**
- **Power Good Output**
- **Output Voltage Accuracy in PWM Mode ±1.5%**
- **Output Capacitor Discharge Function**
- **Typical 18 µA Quiescent Current**
- **100% Duty Cycle for Lowest Dropout**
- **Voltage Positioning**
- **Clock Dithering**
- **Supports Maximum 1mm Height Solutions**
- **Available in a 2x2x0.75mm SON**

APPLICATIONS

- **POL**
- **Notebooks, Pocket PCs**
- **Portable Media Players**
- **DSP Supply**

DESCRIPTION

The TPS6206x is a family of highly efficient synchronous step down DC-DC converters. They provide up to 2.0A output current.

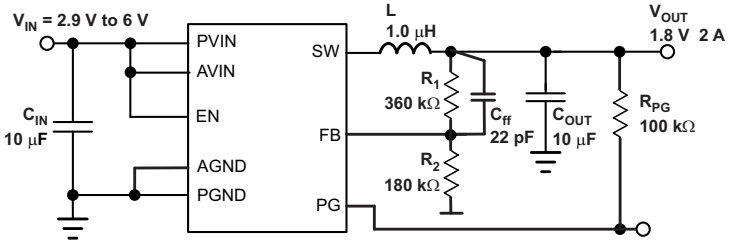
With an input voltage range of 2.9V to 6V the device is a perfect fit for power conversion from a 5V or 3.3V system supply rail. The TPS6206x operates at 3MHz fixed frequency and enters Power Save Mode operation at light load currents to maintain high efficiency over the entire load current range. The Power Save Mode is optimized for low output voltage ripple. For low noise applications, TPS62065 can be forced into fixed frequency PWM mode by pulling the MODE pin high. TPS62067 provides an open drain power good output.

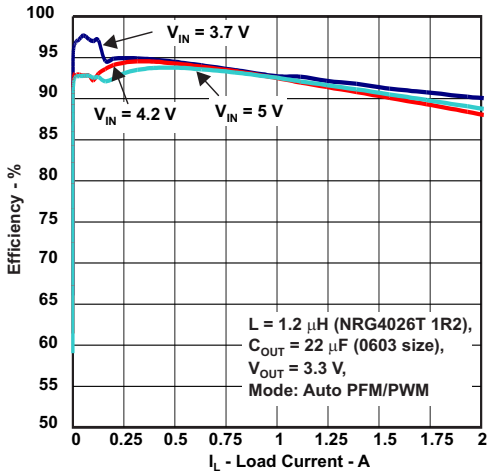
In the shutdown mode, the current consumption is reduced to less than 1µA and an internal circuit discharges the output capacitor.

TPS6206x family is optimized for operation with a tiny 1.0µH inductor and a small 10µF output capacitor to achieve smallest solution size and high regulation performance.

The TPS6206X is available in a small 2x2x0.75mm 8-pin SON package.

TYPICAL APPLICATION CIRCUIT





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PART NUMBER	OUTPUT VOLTAGE(2)	FUNCTION		MAXIMUM OUTPUT CURRENT	PACKAGE DESIGNATOR	ORDERING(3)	PACKAGE MARKING
			MODE	Power Good (PG)				
–40°C to 85°C	TPS62065	Adjustable	Selectable	No	2.0 A	DSG	TPS62065DSG	OFA
	TPS62067	Adjustable	Auto PWM/PFM	Yes	2.0 A	DSG	TPS62067DSG	ODH

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Contact TI for other fixed output voltage options
(3) The DSG (SON-8) packages is available in tape on reel. Add R suffix to order quantities of 3000 parts per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE		UNIT
		MIN	MAX	
Voltage Range (2)	AVIN, PVIN	–0.3	7	V
	EN, MODE, PG, FB	–0.3 to	V_{IN} +0.3 < 7	
	SW	–0.3	7	
Current (sink)	into PG		1	mA
Current (source)	Peak output	Internally limited		A
Electrostatic Discharge (HBM) QSS 009-105 (JESD22-A114A)(3)			2	kV
Electrostatic Discharge (CDM) QSS 009-147 (JESD22-C101B.01)			1	
Electrostatic Discharge (Machine model)			200	V
Temperature	T_J	–40	125	°C
	T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
AV_{IN} , PV_{IN}	Supply voltage	2.9		6	V
	Output current capability			2000	mA
	Output voltage range for adjustable voltage	0.8		VIN	V
L	Effective Inductance Range	0.7	1.0	1.6	µH
C_{OUT}	Effective Output Capacitance Range	4.5	10	22	µF
T_A	Operating ambient temperature(1)	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application (PD(max)), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} – (\theta_{JA} \times P_{D(max)})$

THERMAL INFORMATION

THERMAL METRIC(1)		TPS62065 TPS62067 DSG 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	65.3	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	74.2	
θ_{JB}	Junction-to-board thermal resistance	35.4	
ψ_{JT}	Junction-to-top characterization parameter	2.2	
ψ_{JB}	Junction-to-board characterization parameter	36.0	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	12.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

Over full operating ambient temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN = 3.6V. External components C_{IN} = 10µF 0603, C_{OUT} = 10µF 0603, L = 1.0µH, see the parameter measurement information.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.9		6	V
I_Q	Operating quiescent current	I_{OUT} = 0 mA, device operating in PFM mode and not device not switching		18		µA
I_{SD}	Shutdown current	EN = GND, current into AVIN and PVIN combined		0.1	1	µA
V_{UVLO}	Undervoltage lockout threshold	Falling	1.73	1.78	1.83	V
		Rising	1.9	1.95	1.99	
ENABLE, MODE						
V_{IH}	High level input voltage	2.9 V ≤ V_{IN} ≤ 6 V	1.0		6	V
V_{IL}	Low level input voltage	2.9 V ≤ V_{IN} ≤ 6 V	0		0.4	V
I_{IN}	Input bias current	EN, Mode tied to GND or AVIN		0.01	1	µA
POWER GOOD OPEN DRAIN OUTPUT						
V_{THPG}	Power good threshold voltage	Rising feedback voltage	93%	95%	98%	
		Falling feedback voltage	87%	90%	92%	
V_{OL}	Output low voltage	I_{OUT} = –1mA; must be limited by external pullup resistor (1)			0.3	V
V_H	Output high voltage	Voltage applied to PG pin via external pullup resistor			V_{IN}	V
I_{LKG}	Leakage current into PG pin	$V_{(PG)}$ = 3.6V			100	nA
t_{PGDL}	Internal power good delay time			5		µs
POWER SWITCH						
$R_{DS(on)}$	High-side MOSFET on-resistance	V_{IN} = 3.6 V (1)		120	**180**	mΩ
		V_{IN} = 5.0 V (1)		95	**150**	
$R_{DS(on)}$	Low-side MOSFET on-resistance	V_{IN} = 3.6 V (1)		90	**130**	mΩ
		V_{IN} = 5.0 V (1)		75	**100**	
I_{LIMF}	Forward current limit MOSFET high-side and low-side	2.9V ≤ V_{IN} ≤ 6 V	2300	2750	3300	mA
T_{SD}	Thermal shutdown	Increasing junction temperature		**150**		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		10		
OSCILLATOR						
f_{SW}	Oscillator frequency	2.9 V ≤ V_{IN} ≤ 6 V	2.6	3	3.4	MHz
OUTPUT						

(1) Maximum value applies for T_J = 85°C

ELECTRICAL CHARACTERISTICS (continued)

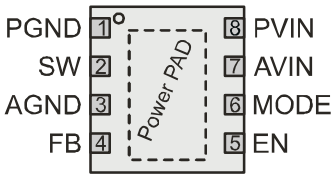
Over full operating ambient temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN = 3.6V. External components C_{IN} = 10µF 0603, C_{OUT} = 10µF 0603, L = 1.0µH, see the parameter measurement information.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ref}	Reference voltage			600		mV
$V_{FB(PWM)}$	Feedback voltage PWM Mode	PWM operation, MODE = V_{IN} , 2.9 V ≤ V_{IN} ≤ 6 V, 0 mA load	–1.5	0	1.5	%
$V_{FB(PFM)}$	Feedback voltage PFM mode, Voltage Positioning	device in PFM mode, voltage positioning active(2)		1		
V_{FB}	Load regulation			-0.5		%/A
	Line regulation			0		%/V
$R_{(Discharge)}$	Internal discharge resistor	Activated with EN = GND, 2.9V ≤ V_{IN}≤ 6V, 0.8 ≤ V_{OUT}≤ 3.6V	75	200	1450	Ω
t_{START}	Start-up time	Time from active EN to reach 95% of V_{OUT}		500		µs

(2) In PFM mode, the internal reference voltage is set to typ. 1.01×V_{ref}. See the parameter measurement information.

PIN ASSIGNMENTS

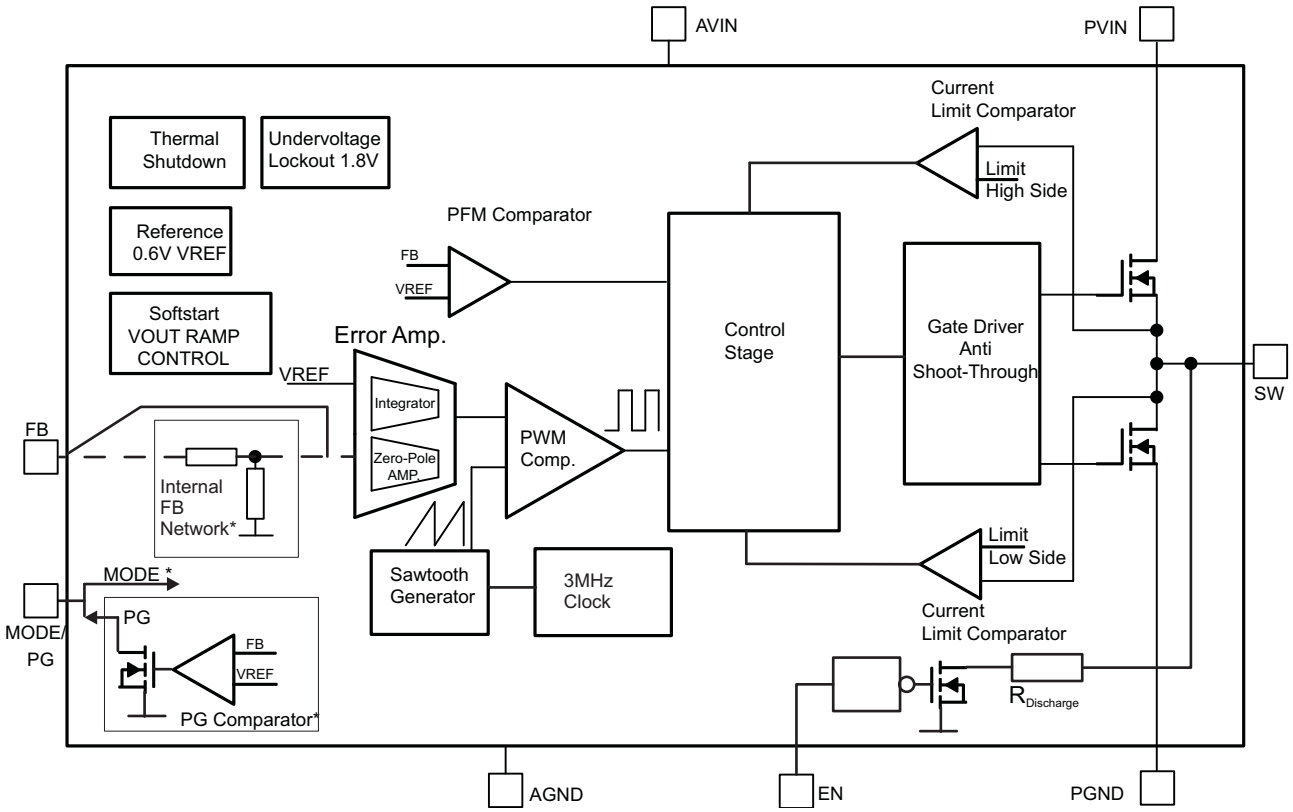
DSG PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

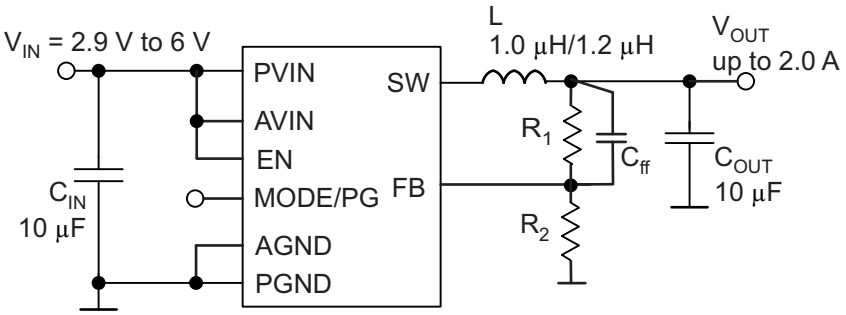
TERMINAL		I/O	DESCRIPTION
NAME	NO. SON 2x2-8		
PGND	1	PWR	GND supply pin for the output stage.
SW	2	OUT	This is the switch pin and is connected to the internal MOSFET switches. Connect the external inductor between this terminal and the output capacitor.
AGND	3	IN	Analog GND supply pin for the control circuit.
FB	4	IN	Feedback pin for the internal regulation loop. Connect the external resistor divider to this pin. In case of fixed output voltage option, connect this pin directly to the output capacitor
EN	5	IN	This is the enable pin of the device. Pulling this pin to low forces the device into shutdown mode. Pulling this pin to high enables the device. This pin must be terminated
MODE	6	IN	**MODE**: MODE pin = high forces the device to operate in fixed frequency PWM mode. MODE pin = low enables the Power Save Mode with automatic transition from PFM mode to fixed frequency PWM mode. This pin must be terminated.
PG		Open Drain	**PG**: Power Good Open Drain output. Connect an external pull up resistor to a rail which is below or equal AV_{IN}.
AV_{IN}	7	IN	Analog V_{IN} power supply for the control circuit. Need to be connected to PVIN and input capacitor.
PV_{IN}	8	PWR	V_{IN} power supply pin for the output stage.
Power PAD			For good thermal performance, this PAD must be soldered to the land pattern on the pcb. This PAD should be used as device GND.

FUNCTIONAL BLOCK DIAGRAM



* Function depends on device option

PARAMETER MEASUREMENT INFORMATION



L: LQH44PN1R0NP0, L = 1.0 µH,Murata,
NRG4026T1R2, L = 1.2 µH, Taiyo Yuden
C_{IN}/C_{OUT}: GRM188R60J106U, Murata 0603 size

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS			FIGURE
η	Efficiency	Load Current, V_{OUT} = 1.2 V, Auto PF//PWM Mode, Linear Scale	Figure 1
		Load Current, V_{OUT} = 1.8 V, Auto PFM/PWM Mode, Linear Scale	Figure 2
		Load Current, V_{OUT} = 3.3 V, PFM/PWM Mode, Linear Scale	Figure 3
		Load Current, V_{OUT} = 1.8 V, Auto PFM/PWM Mode vs. Forced PWM Mode, Logarithmic Scale	Figure 4
	Output Voltage Accuracy	Load Current, V_{OUT} = 1.8 V, Auto PFM/PWM Mode	Figure 5
		Load Current, V_{OUT} = 1.8 V, Forced PWM Mode	Figure 6
	Shutdown Current	Input Voltage and Ambient Temperature	Figure 7
	Quiescent Current	Input Voltage	Figure 8
	Oscillator Frequency	Input Voltage	Figure 9
	Static Drain-Source On-State Resistance	Input Voltage, Low-Side Switch	Figure 10
		Input Voltage, High-Side Switch	Figure 11
	$R_{DISCHARGE}$	Input Voltage vs. V_{OUT}	Figure 12
	Typical Operation	PWM Mode, V_{IN} = 3.6 V, V_{OUT} = 1.8 V, 500 mA, L = 1.2 µH, C_{OUT} = 10µF	Figure 13
		PFM Mode, V_{IN} = 3.6 V, V_{OUT} = 1.8 V, 20 mA, L = 1.2 µH, C_{OUT} = 10µF	Figure 14
	Load Transient	PWM Mode, V_{IN} = 3.6 V, V_{OUT} = 1.2 V, 0.2 mA to 1 A	Figure 15
		PFM Mode, V_{IN} = 3.6 V, V_{OUT} = 1.2 V, 20 mA to 250 mA	Figure 16
		V_{IN} = 3.6 V, V_{OUT} = 1.8 V, 200 mA to 1500 mA	Figure 17
	Line Transient	PWM Mode, V_{IN} = 3.6 V to 4.2 V, V_{OUT} = 1.8 V, 500 mA	Figure 18
		PFM Mode, V_{IN} = 3.6 V to 4.2 V, V_{OUT} = 1.8 V, 500 mA	Figure 19
	Startup into Load	V_{IN} = 3.6 V, V_{OUT} = 1.8 V, Load = 2.2-Ω	Figure 20
	Startup TPS62067	Into 2.2-Ω Load with Power Good	Figure 21
	Output Discharge	V_{IN} = 3.6 V, V_{OUT} = 1.8 V, No Load	Figure 22
	Shutdown TPS62067	V_{IN} = 4.2 V, V_{OUT} = 3.3 V, No Load, PG Pullup Resistor 10 kΩ	Figure 23

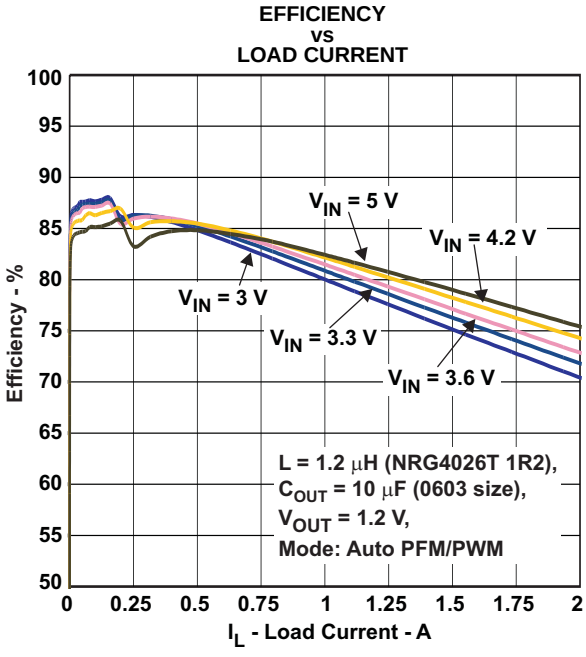


Figure 1. V_{OUT} = 1.2V, Auto PFM/PWM Mode, Linear Scale

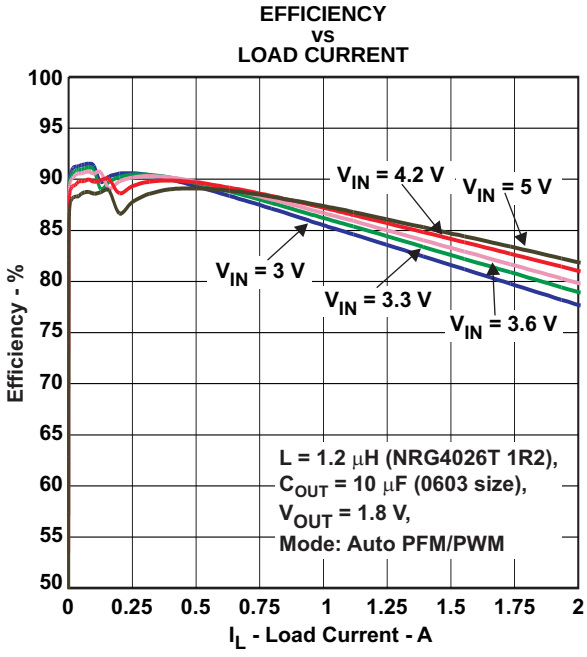


Figure 2. V_{OUT} = 1.8V, Auto PFM/PWM Mode, Linear Scale

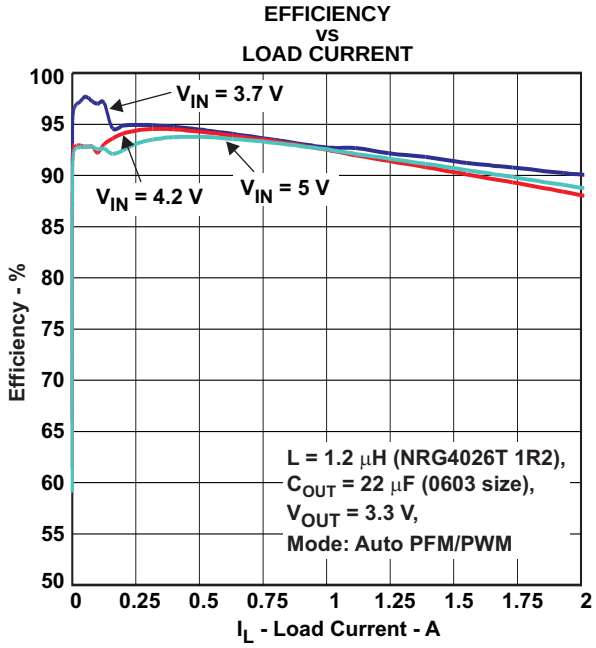


Figure 3. V_{OUT} = 3.3V, Auto PFM/PWM Mode, Linear Scale

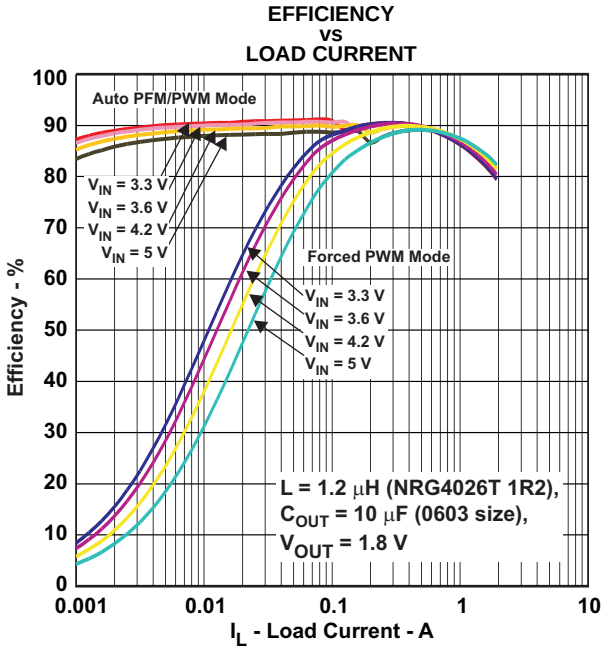


Figure 4. Auto PFM/PWM Mode vs. Forced PWM Mode, Logarithmic Scale

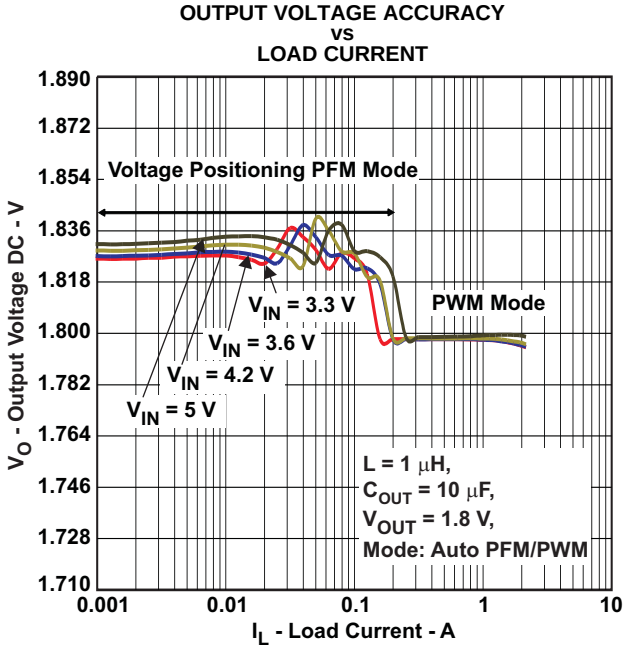


Figure 5. Auto PFM/PWM Mode

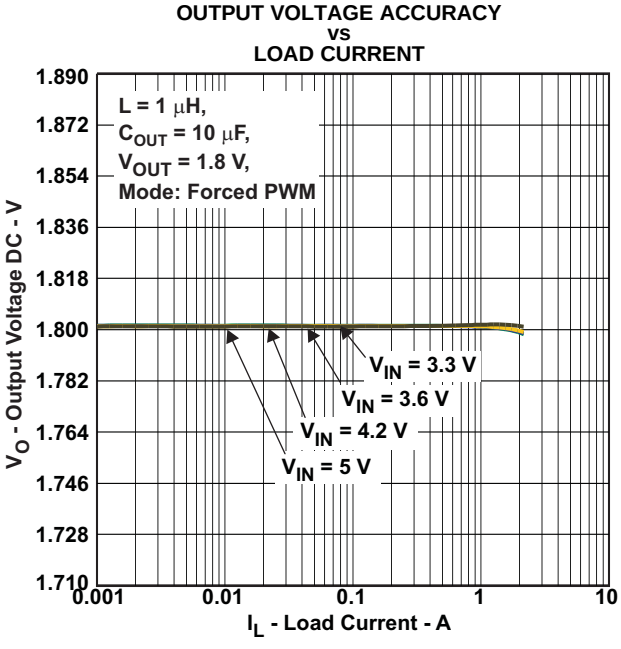


Figure 6. Forced PWM Mode

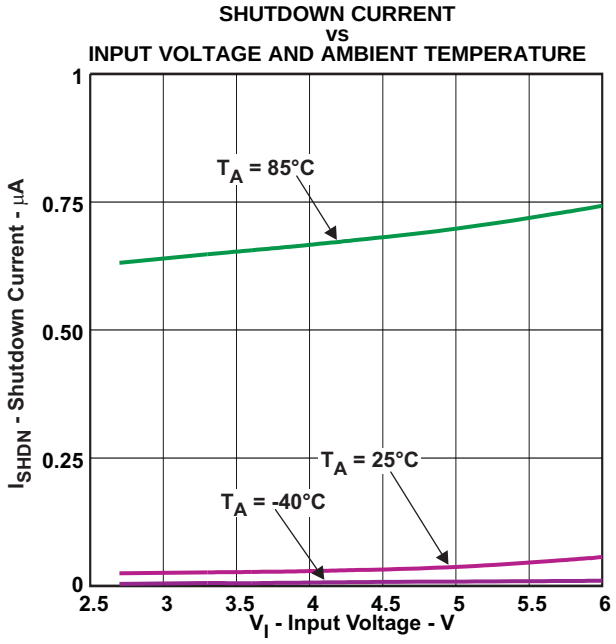


Figure 7.

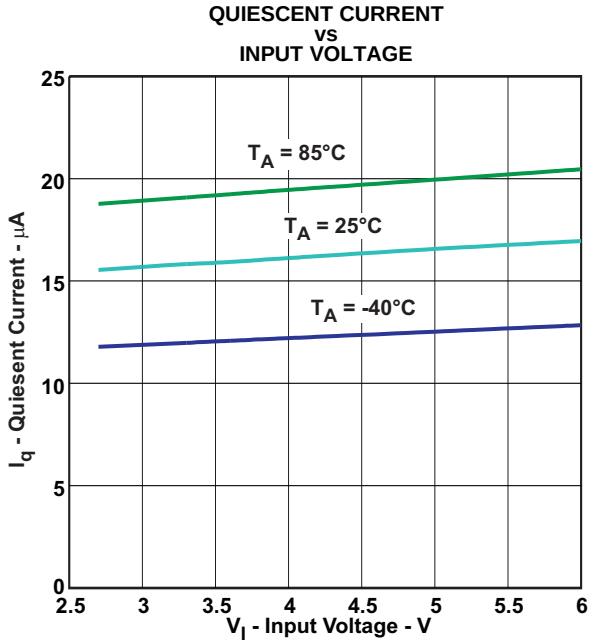


Figure 8.

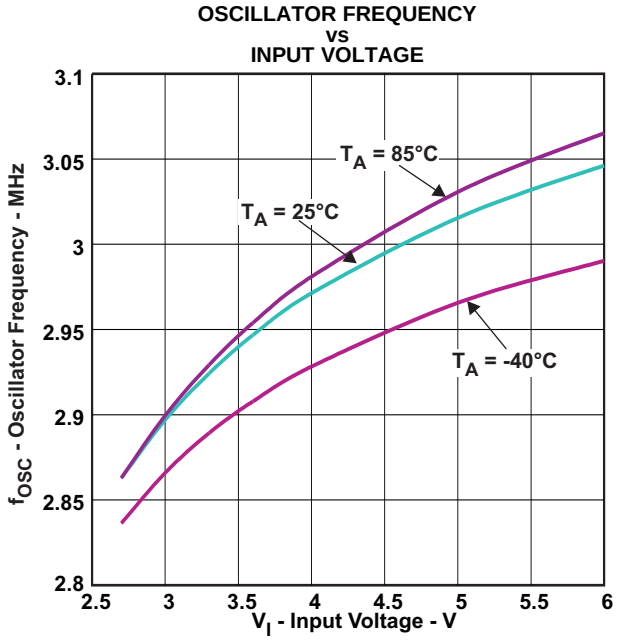


Figure 9.

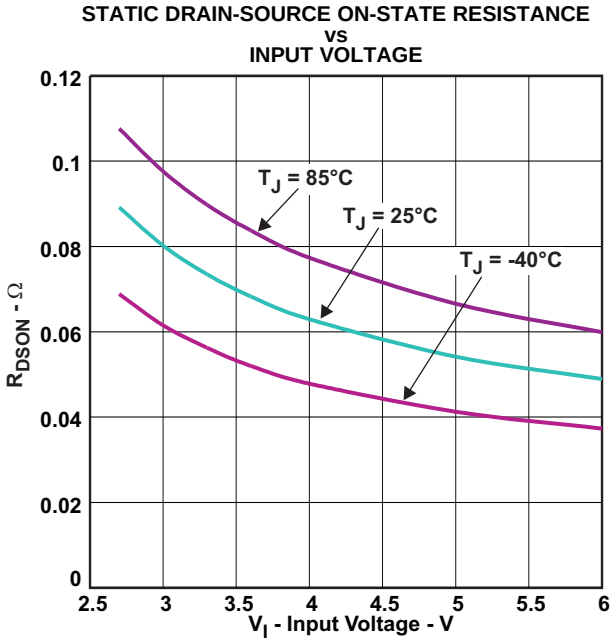


Figure 10. Low-Side Switch

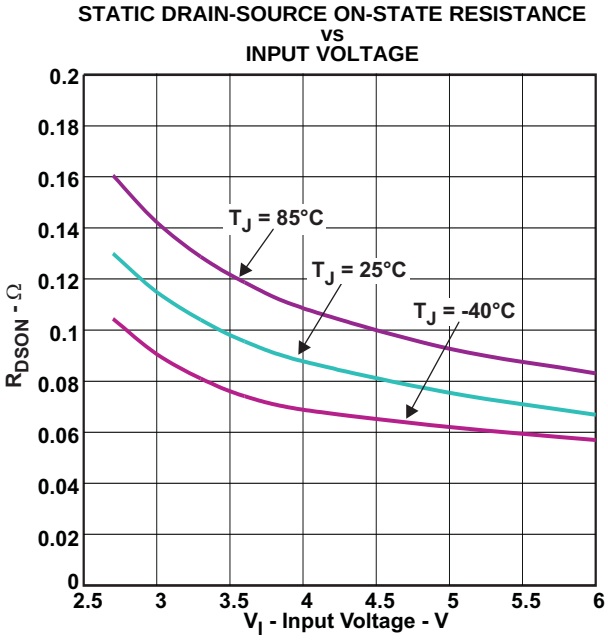


Figure 11. High-Side Switch

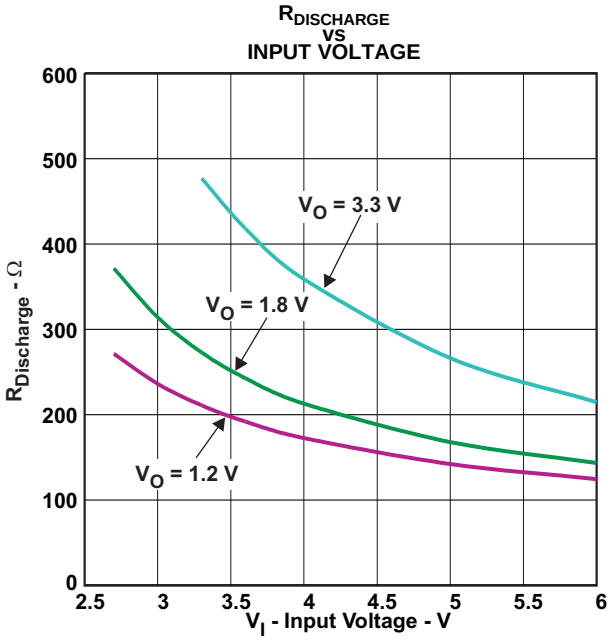


Figure 12.

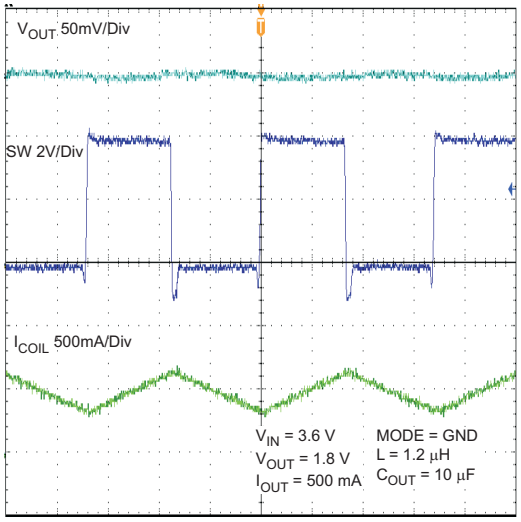


Figure 13. Typical Operation (PWM Mode)

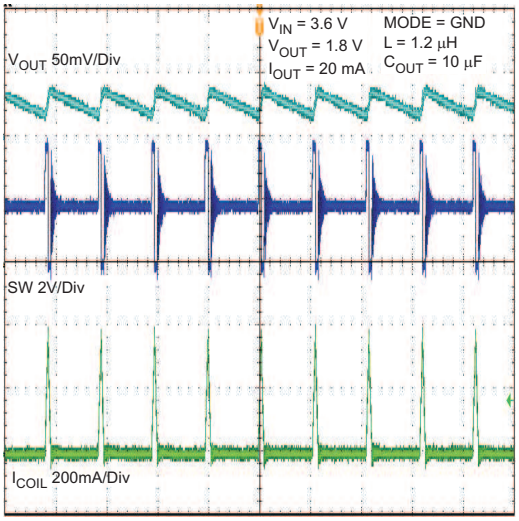
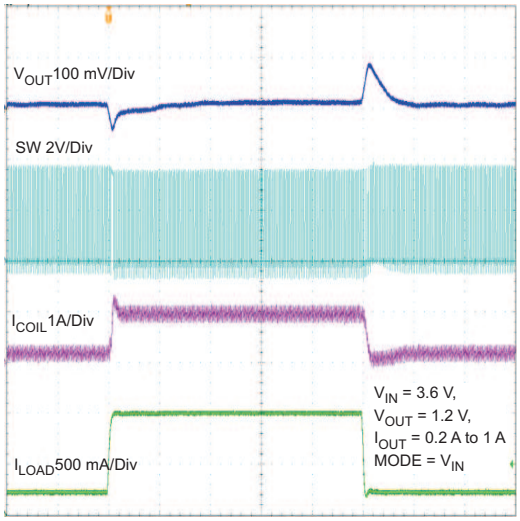
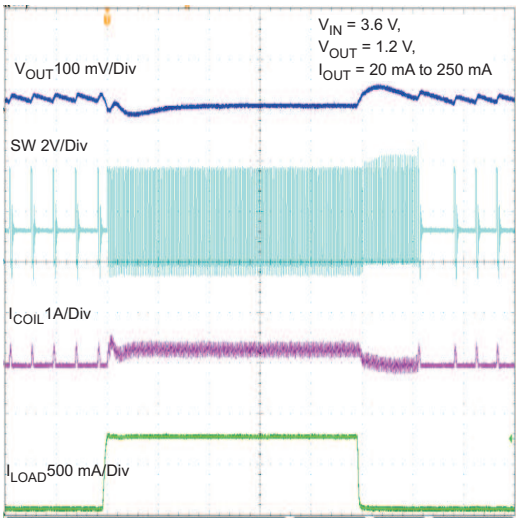


Figure 14. Typical Operation (PFM Mode)



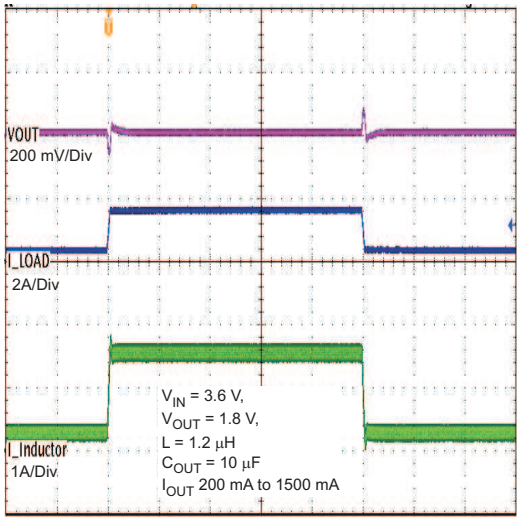
Time Base - 10 µs/Div

Figure 15. Load Transient Response PWM Mode 0.2A To 1A



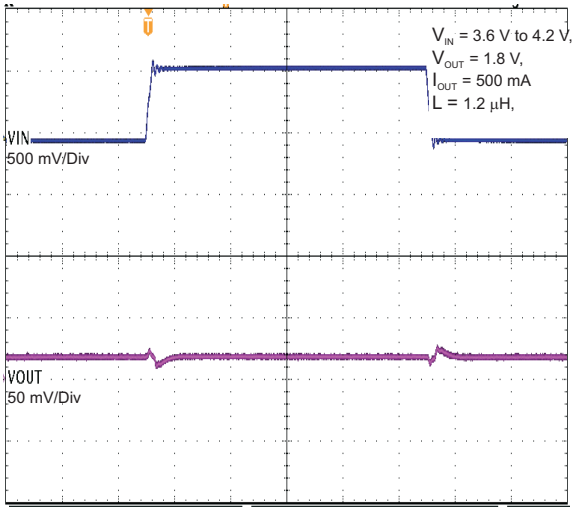
Time Base - 10 µs/Div

Figure 16. Load Transient PFM Mode 20 mA to 250mA



Time Base - 100µs/Div

Figure 17. Load Transient Response 200 mA To 1500 mA



Time Base - 100 µs/Div

Figure 18. Line Transient Response PWM Mode

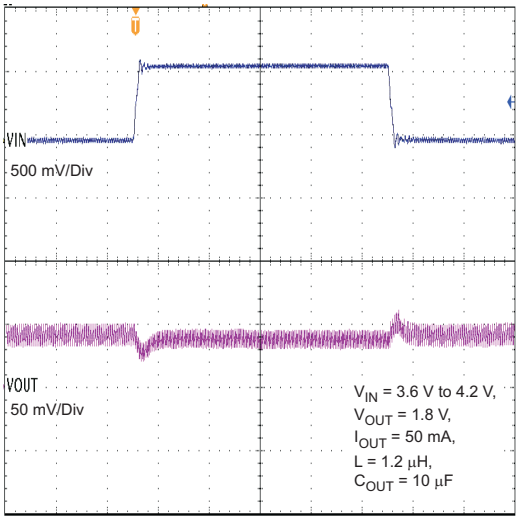


Figure 19. Line Transient PFM Mode

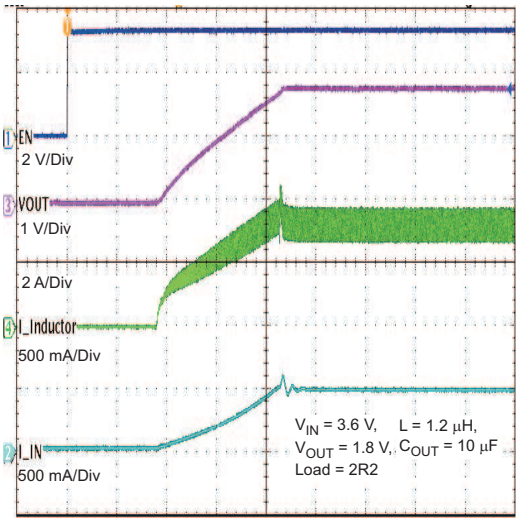


Figure 20. Startup Into Load – V_{OUT} 1.8V

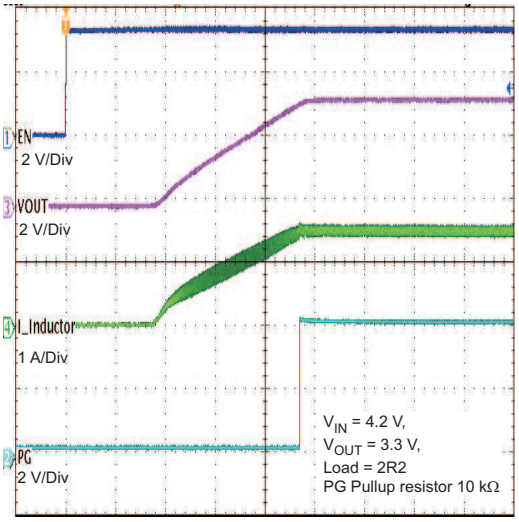


Figure 21. Startup TPS62067 into 2.2-Ω Load with Power Good

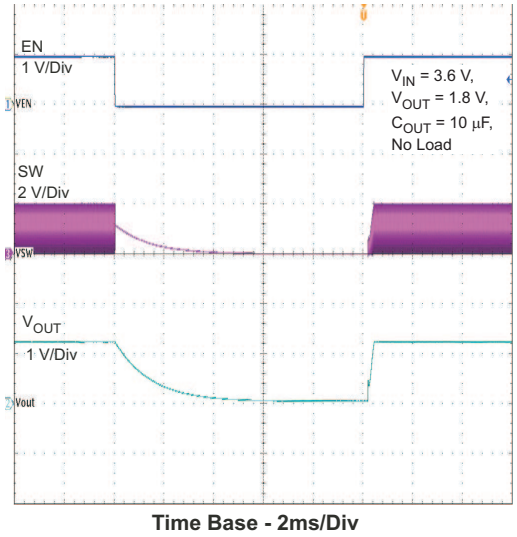
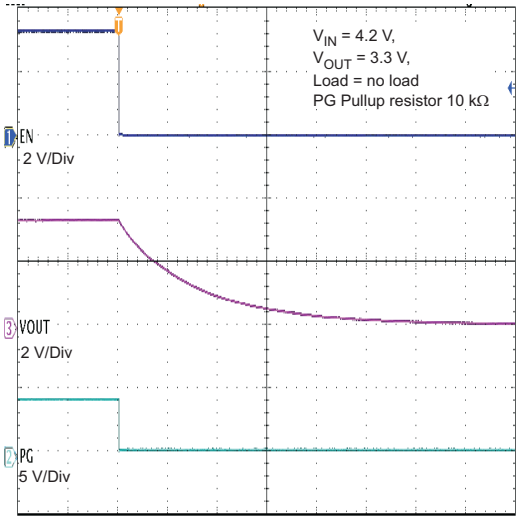


Figure 22. Output Discharge



Time Base - 1 ms/Div

Figure 23. Shutdown TPS62067

DETAILED DESCRIPTION

OPERATION

The TPS6206x step down converter operates with typically 3MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents the converter can automatically enter Power Save Mode and operates then in PFM (Pulse Frequency Mode) mode.

During PWM operation the converter use a unique fast response voltage mode controller scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the High Side MOSFET switch is turned on. The current flows now from the input capacitor via the High Side MOSFET switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic will turn off the switch. The current limit comparator will also turn off the switch in case the current limit of the High Side MOSFET switch is exceeded. After a dead time preventing shoot through current, the Low Side MOSFET rectifier is turned on and the inductor current ramps down. The current flows now from the inductor to the output capacitor and to the load. It returns back to the inductor through the Low Side MOSFET rectifier..

The next cycle will be initiated by the clock signal again turning off the Low Side MOSFET rectifier and turning on the High Side MOSFET switch.

POWER SAVE MODE

At TPS62065 pulling the Mode pin low enables Power Save Mode. In TPS62067 Power Save Mode is enabled per default. If the load current decreases, the converter enters Power Save Mode operation automatically. During Power Save Mode the converter skips switching and operates with reduced frequency in PFM mode with a minimum quiescent current to maintain high efficiency. The converter positions the output voltage typically +1% above the nominal output voltage. This voltage positioning feature minimizes voltage drops caused by a sudden load step.

The transition from PWM mode to PFM mode occurs once the inductor current in the Low Side MOSFET switch becomes zero, which indicates discontinuous conduction mode.

During the Power Save Mode the output voltage is monitored with a PFM comparator. As the output voltage falls below the PFM comparator threshold of $V_{OUTnominal}$ +1%, the device starts a PFM current pulse. For this the High Side MOSFET switch will turn on and the inductor current ramps up. After the On-time expires the switch will be turned off and the Low Side MOSFET switch will be turned on until the inductor current becomes zero.

The converter effectively delivers a current to the output capacitor and the load. If the load is below the delivered current the output voltage will rise. If the output voltage is equal or higher than the PFM comparator threshold, the device stops switching and enters a sleep mode with typ. 18µA current consumption.

In case the output voltage is still below the PFM comparator threshold, further PFM current pulses will be generated until the PFM comparator threshold is reached. The converter starts switching again once the output voltage drops below the PFM comparator threshold due to the load current.

The PFM mode is exited and PWM mode entered in case the output current can no longer be supported in PFM mode.

Dynamic Voltage Positioning

This feature reduces the voltage under/overshoots at load steps from light to heavy load and vice versa. It is active in Power Save Mode and regulates the output voltage 1% higher than the nominal value. This provides more headroom for both the voltage drop at a load step, and the voltage increase at a load throw-off.

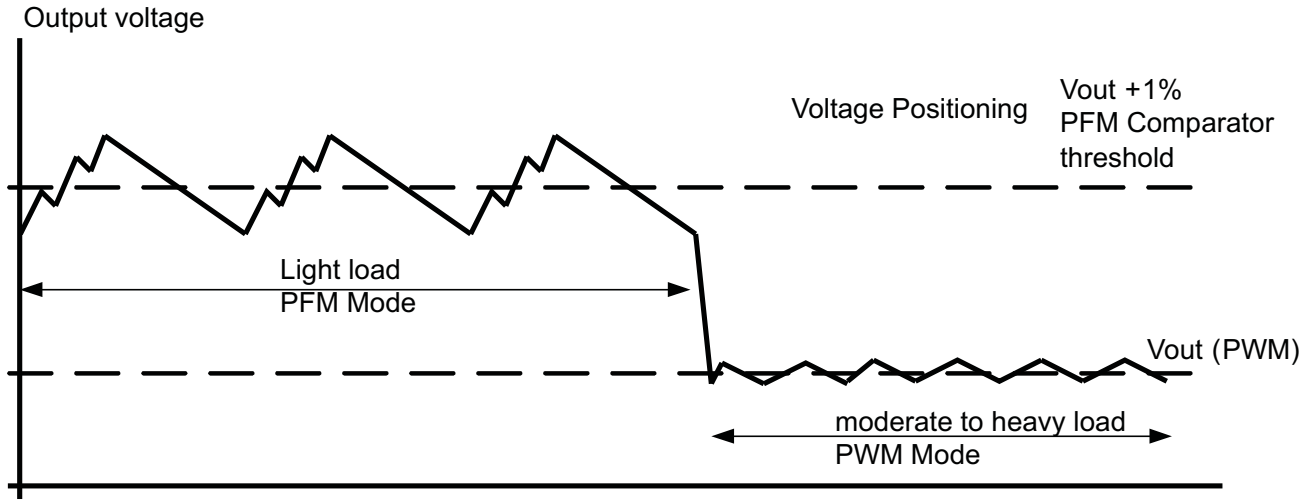


Figure 24. Power Save Mode Operation with automatic Mode transition

100% Duty Cycle Low Dropout Operation

The device starts to enter 100% duty cycle mode as the input voltage comes close to the nominal output voltage. In order to maintain the output voltage, the High-Side MOSFET switch is turned on 100% for one or more cycles.

With further decreasing VIN the High-Side MOSFET switch is turned on completely. In this case the converter offers a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range.

The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$$V_{IN}min = V_O max + I_O max \times (R_{DS(on)} max + R_L)$$

With:

$I_O$max = maximum output current

$R_{DS(on)}$max = maximum P-channel switch $R_{DS(on)}$.

R_L = DC resistance of the inductor

$V_O$max = nominal output voltage plus maximum output voltage tolerance

Undervoltage Lockout

The under voltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery. It disables the output stage of the converter once the falling VIN trips the under-voltage lockout threshold V_{UVLO}. The under-voltage lockout threshold V_{UVLO} for falling V_{IN} is typically 1.78V. The device starts operation once the rising V_{IN} trips under-voltage lockout threshold V_{UVLO} again at typically 1.95V.

Output Capacitor Discharge

With EN = GND, the device enters shutdown mode and all internal circuits are disabled. The SW pin is connected to PGND via an internal resistor to discharge the output capacitor. This feature ensures a startup in a discharged output capacitor once the converter is enabled again and prevents "floating" charge on the output capacitor. The output voltage ramps up monotonic starting from 0V.

MODE SELECTION (TPS62065)

The MODE pin allows mode selection between forced PWM mode and Power Save Mode.

Connecting this pin to GND enables the Power Save Mode with automatic transition between PWM and PFM mode. Pulling the MODE pin high forces the converter to operate in fixed frequency PWM mode even at light load currents. This allows simple filtering of the switching frequency for noise sensitive applications. In this mode, the efficiency is lower compared to the power save mode during light loads.

The condition of the MODE pin can be changed during operation and allows efficient power management by adjusting the operation mode of the converter to the specific system requirements.

In device options where the MODE Pin is replaced with Power Good output, the Power Save Mode is enabled per default.

POWER GOOD OUTPUT (TPS62067)

This function is available in the TPS62067. The Power Good Output is an open-drain output and requires an external pull-up resistor. The circuit is active once the device is enabled and AVIN is above the undervoltage lockout threshold V_{UVLO}. It is driven by an internal comparator connected to the FB voltage. The PG output provides a high level once the feedback voltage exceeds typically 95% of its nominal value. The PG output is driven to low level once the feedback voltage falls below typically 90% of its nominal value. The PG output is activated with an internal delay of 5µs.

The PG open-drain output transistor is turned on immediately with EN = low level and pulls the output low. The external pull up resistor can be connected to any voltage rail lower or equal the voltage applied to AV_{IN} of the device. The value of the pull-up resistor must be carefully selected in order to limit the current into the PG pin to maximum 1.0mA. The external pull up resistor can be connected to VOUT or another voltage rail which does not exceed the VIN level. The current flowing through the pull up resistor impacts the current consumption of the application circuit in shutdown mode.

The shut down current of the device does not include the current through the external pull-up and internal open-drain stage. The PG signal can be used for sequencing various converters or to reset a microcontroller.

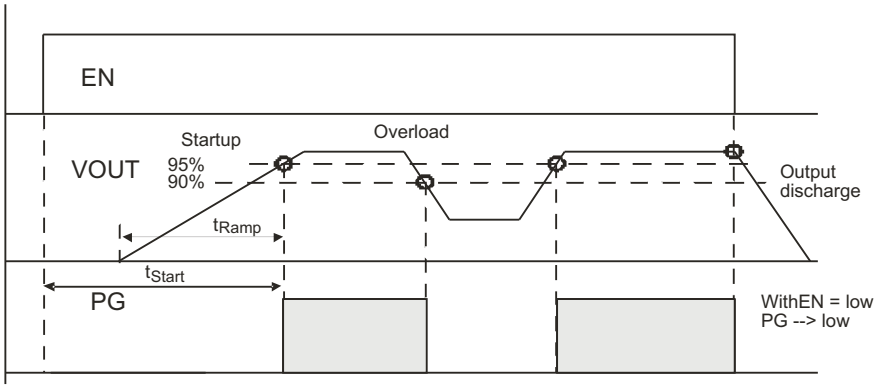


Figure 25. Power Good Output PG

ENABLE

The device is enabled by setting EN pin to high. At first, the internal reference is activated and the internal analog circuits are settled. Afterwards, the soft start is activated and the output voltage is ramped up. The output voltages reaches 95% of its nominal value within $t_{START}$of typically 500 µs after the device has been enabled. The EN input can be used to control power sequencing in a system with various DC/DC converters. The EN pin can be connected to the output of another converter, to drive the EN pin high and getting a sequencing of supply rails. With EN = GND, the device enters shutdown mode. In this mode, all circuits are disabled and the SW pin is connected to PGND via an internal resistor to discharge the output.

SOFT START

The TPS6206x has an internal soft start circuit that controls the ramp up of the output voltage. Once the converter is enabled and the input voltage is above the undervoltage lockout threshold $V_{UVLO}$the output voltage ramps up from 5% to 95% of its nominal value within t_{Ramp} of typ. 250µs.

This limits the inrush current in the converter during start up and prevents possible input voltage drops when a battery or high impedance power source is used.

During soft start, the switch current limit is reduced to 1/3 of its nominal value ILIMF until the output voltage reaches 1/3 of its nominal value. Once the output voltage trips this threshold, the device operates with its nominal current limit I_{LIMF}.

INTERNAL CURRENT LIMIT / FOLD-BACK CURRENT LIMIT FOR SHORT-CIRCUIT PROTECTION

During normal operation the High-Side and Low-Side MOSFET switches are protected by its current limits I_{LIMF}. Once the High-Side MOSFET switch reaches its current limit, it is turned off and the Low-Side MOSFET switch is turned on. The High-Side MOSFET switch can only turn on again, once the current in the Low -Side MOSFET switch decreases below its current limit I_{LIMF}. The device is capable to provide peak inductor currents up to its internal current limit $_{ILIMF.}$.

As soon as the switch current limits are hit and the output voltage falls below 1/3 of the nominal output voltage due to overload or short circuit condition, the foldback current limit is enabled. In this case the switch current limit is reduced to 1/3 of the nominal value I_{LIMF}.

Due to the short-circuit protection is enabled during start-up, the device does not deliver more than 1/3 of its nominal current limit I_{LIMF} until the output voltage exceeds 1/3 of the nominal output voltage. This needs to be considered when a load is connected to the output of the converter, which acts as a current sink.

CLOCK DITHERING

In order to reduce the noise level of switch frequency harmonics in the higher RF bands, the TPS6206x family has a built-in clock-dithering circuit. The oscillator frequency is slightly modulated with a sub clock causing a clock dither of typ. 6ns.

THERMAL SHUTDOWN

As soon as the junction temperature, T_J, exceeds 150°C (typical) the device goes into thermal shutdown. In this mode, the High-Side and Low-Side MOSFETs are turned off. The device continues its operation with a softstart once the junction temperature falls below the thermal shutdown hysteresis.

APPLICATION INFORMATION

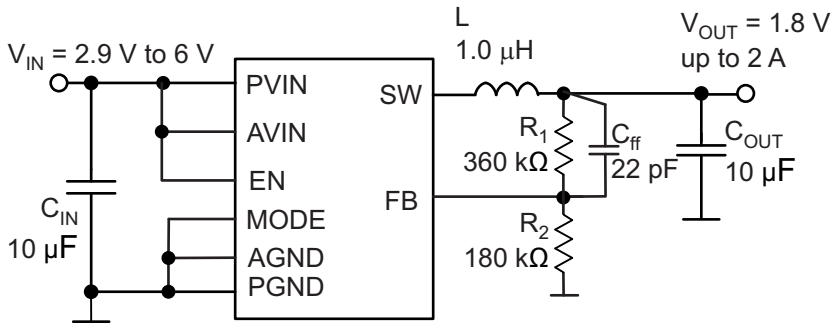


Figure 26. TPS62065 1.8V Adjustable Output Voltage Configuration

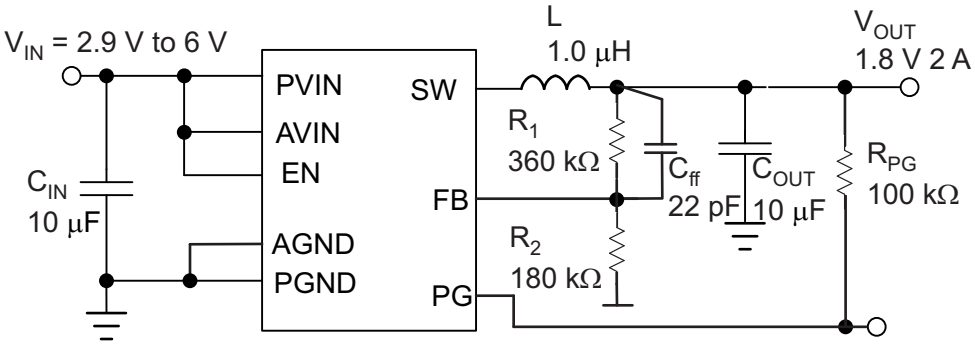


Figure 27. TPS62067 Adjustable 1.8-V Output

OUTPUT VOLTAGE SETTING

The output voltage can be calculated to:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \qquad R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_2$$

with an internal reference voltage V_{REF} typically 0.6V.

To minimize the current through the feedback divider network, R_2 should be within the range of 120 kΩ to 360 kΩ. The sum of R_1 and R_2 should not exceed ~1MΩ, to keep the network robust against noise. An external feed-forward capacitor C_{ff} is required for optimum regulation performance. Lower resistor values can be used. R_1 and C_{ff} places a zero in the loop. The right value for C_{ff} can be calculated as:

$$f_z = \frac{1}{2 \times \pi \times R_1 \times C_{ff}} = 25\ \text{kHz}$$

$$C_{ff} = \frac{1}{2 \times \pi \times R_1 \times 25\ \text{kHz}}$$

OUTPUT FILTER DESIGN (INDUCTOR AND OUTPUT CAPACITOR)

The internal compensation network of TPS6206x is optimized for a LC output filter with a corner frequency of:

$$f_c = \frac{1}{2 \times \pi \times \sqrt{(1\mu H \times 10\mu F)}} = 50kHz$$

The part operates with nominal inductors of 1.0µH to 1.2 µH and with 10µF to 22µF small X5R and X7R ceramic capacitors. Please refer to the lists of inductors and capacitors. The part is optimized for a 1.0µH inductor and 10µF output capacitor.

Inductor Selection

The inductor value has a direct effect on the ripple current. The selected inductor has to be rated for its dc resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_I or V_O.

Equation 1 calculates the maximum inductor current in PWM mode under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 2. This is recommended because during heavy load transient the inductor current rises above the calculated value.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \quad (1)$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \quad (2)$$

With:

f = Switching Frequency (3MHz typical)

L = Inductor Value

ΔI_L = Peak-to-Peak inductor ripple current

I_{Lmax} = Maximum Inductor current

A more conservative approach is to select the inductor current rating just for the switch current limit $I_{LIMF}$of the converter.

The total losses of the coil have a strong impact on the efficiency of the DC/DC conversion and consist of both the losses in the dc resistance $R_{(DC)}$ and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

Table 1. List of Inductors

DIMENSIONS [mm^3]	INDUCTANCE µH	INDUCTOR TYPE	SUPPLIER
3.2 x 2.5 x 1.0 max	1.0	LQM32PN (MLCC)	Murata
3.7 x 4 x 1.8 max	1.0	LQH44 (wire wound)	Murata
4.0 x 4.0 x 2.6 max	1.2	NRG4026T (wire wound)	Taiyo Yuden
3.5 x 3.7 x 1.8 max	1.2	DE3518 (wire wound)	TOKO

Output Capacitor Selection

The advanced fast-response voltage mode control scheme of the TPS6206x allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies and may not be used. For most applications a nominal 10µF or 22µF capacitor is suitable. At small ceramic capacitors, the DC-bias effect decreases the effective capacitance. Therefore a 22µF capacitor can be used for output voltages higher than 2V, see list of capacitors.

In case additional ceramic capacitors in the supplied system are connected to the output of the DC/DC converter, the output capacitor C_{OUT} need to be decreased in order not to exceed the recommended effective capacitance range. In this case a loop stability analysis must be performed as described later.

At nominal load current, the device operates in PWM mode and the RMS ripple current is calculated as:

$$I_{RMSCout} = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (3)$$

Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. For most applications a 10µF ceramic capacitor is recommended. The input capacitor can be increased without any limit for better input voltage filtering.

Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or VIN step on the input can induce ringing at the V_{IN} pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part by exceeding the maximum ratings.

Table 2. List of Capacitors

CAPACITANCE	TYPE	SIZE [mm^3]	SUPPLIER
10µF	GRM188R60J106M	0603: 1.6 x 0.8 x 0.8	Murata
22µF	GRM188R60G226M	0603: 1.6 x 0.8 x 0.8	Murata
22µF	CL10A226MQ8NRNC	0603: 1.6 x 0.8 x 0.8	Samsung
10µF	CL10A106MQ8NRNC	0603: 1.6 x 0.8 x 0.8	Samsung

CHECKING LOOP STABILITY

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signal

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or wrong L-C output filter combinations. As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turn on of the P-channel MOSFET, the output capacitor must supply all of the current required by the load. V_{OUT} immediately shifts by an amount equal to $\Delta_{I(LOAD)}$ x ESR, where ESR is the effective series resistance of C_{OUT}. $\Delta_{I(LOAD)}$ begins to charge or discharge C_O generating a feedback error signal used by the regulator to return VOUT to its steady-state value. The results are most easily interpreted when the device operates in PWM mode at medium to high load currents.

During this recovery time, V_{OUT} can be monitored for settling time, overshoot, or ringing; that helps evaluate stability of the converter. Without any ringing, the loop has usually more than 45° of phase margin.

LAYOUT CONSIDERATIONS

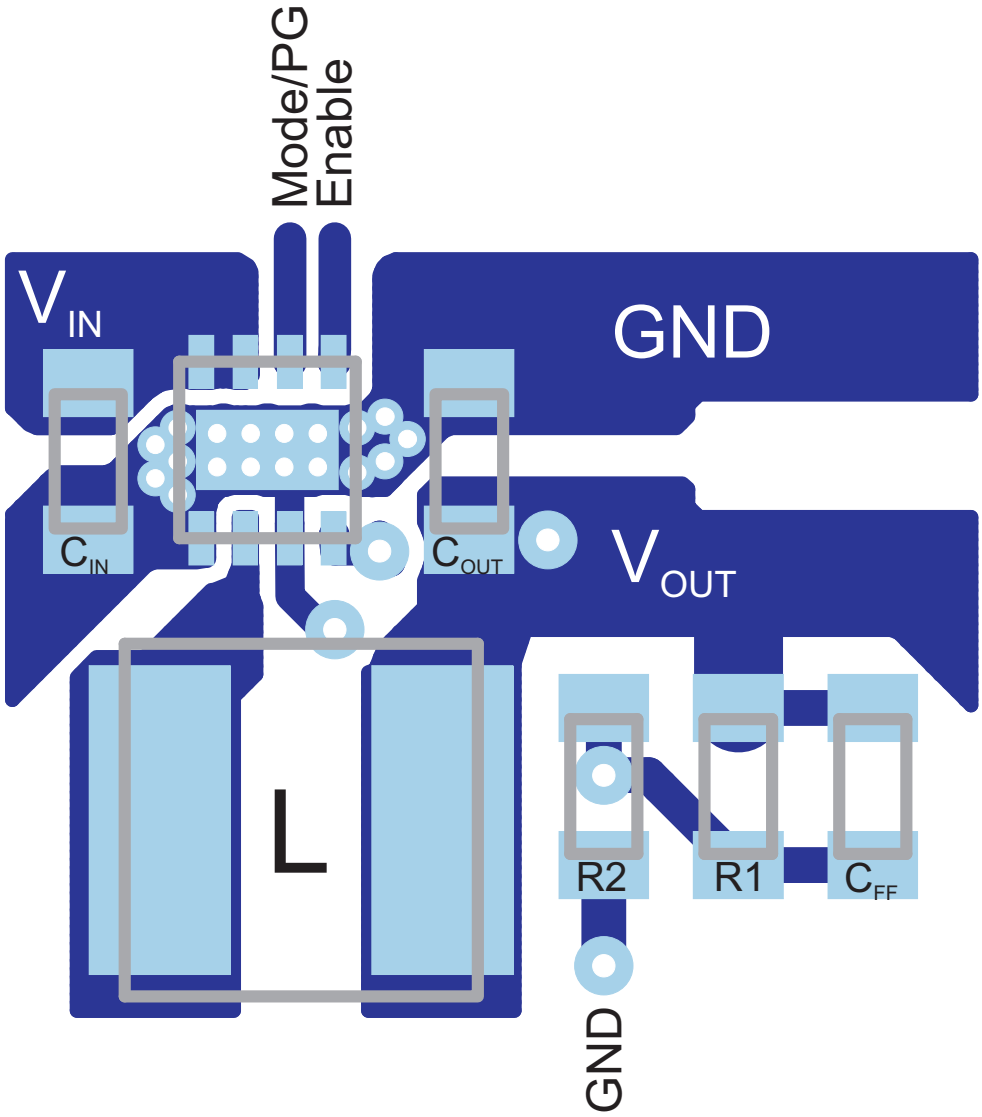


Figure 28. PCB Layout

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues as well as EMI and thermal problems. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor.

Connect the AGND and PGND Pins of the device to the PowerPAD™ land of the PCB and use this pad as a star point. Use a common Power PGND node and a different node for the Signal AGND to minimize the effects of ground noise. The FB divider network should be connected right to the output capacitor and the FB line must be routed away from noisy components and traces (e.g., SW line).

Due to the small package of this converter and the overall small solution size the thermal performance of the PCB layout is important. To get a good thermal performance a four or more Layer PCB design is recommended. The PowerPAD of the IC must be soldered on the power pad area on the PCB to get a proper thermal connection. For good thermal performance the PowerPAD on the PCB needs to be connected to an inner GND plane with sufficient via connections. Please refer to the documentation of the evaluation kit.

REVISION HISTORY

NOTE: Page numbers of previous versions may differ from current version.

Changes from Revision A (May 2010) to Revision B	Page
• Added Thermal Information table and deleted Dissipation Ratings table	3

Changes from Original (March 2010) to Revision A	Page
• Changed V_{IN} Range from "3V to 6V" to "2.9V to 6V", throughout	1
• Added equation to "Output Voltage Setting" section.	17
• Changed equation for calculating $f_{z.}$	17
• Changed equation for calculating $C_{ff.}$	17

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62065DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OFA	Samples
TPS62065DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OFA	Samples
TPS62067DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ODH	Samples
TPS62067DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ODH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

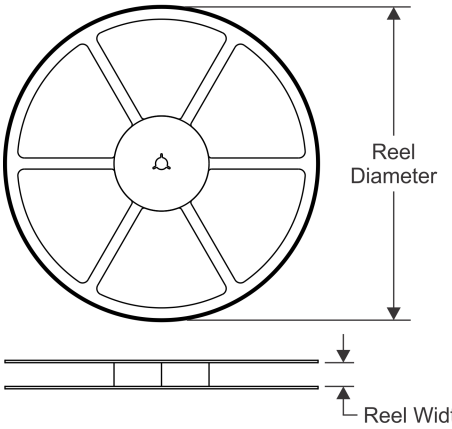
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

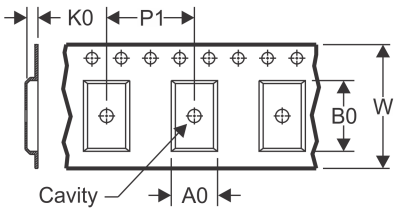
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

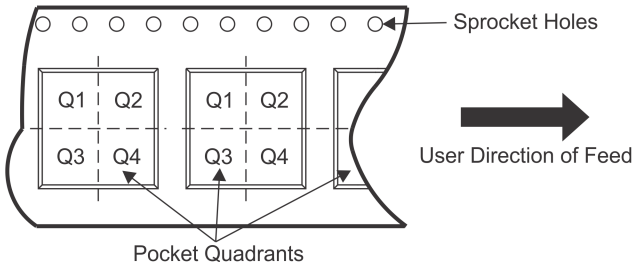


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

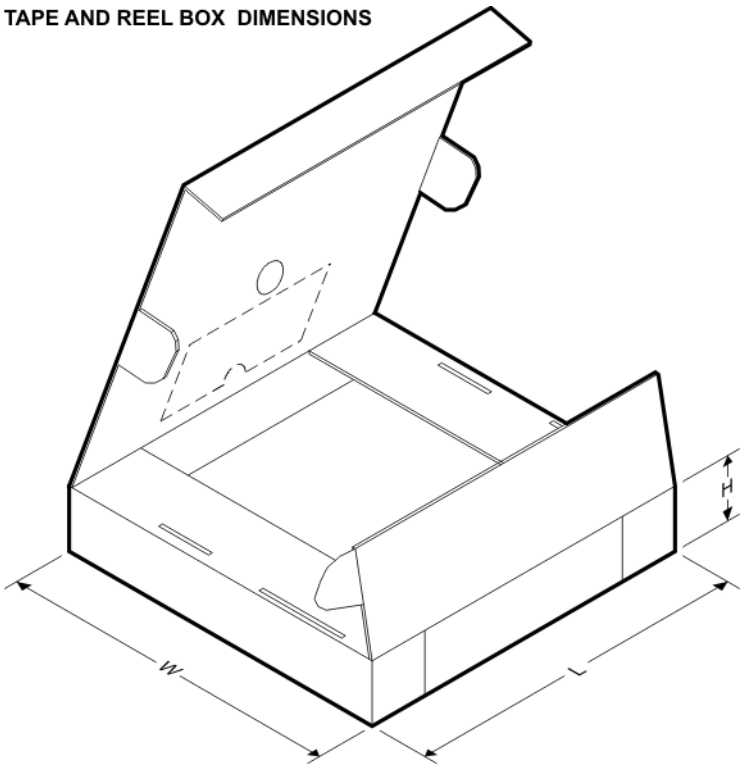
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62065DSGR	WSON	DSG	8	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62065DSGR	WSON	DSG	8	3000	330.0	12.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62065DSGT	WSON	DSG	8	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62065DSGT	WSON	DSG	8	250	180.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62067DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62067DSGR	WSON	DSG	8	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62067DSGT	WSON	DSG	8	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62067DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

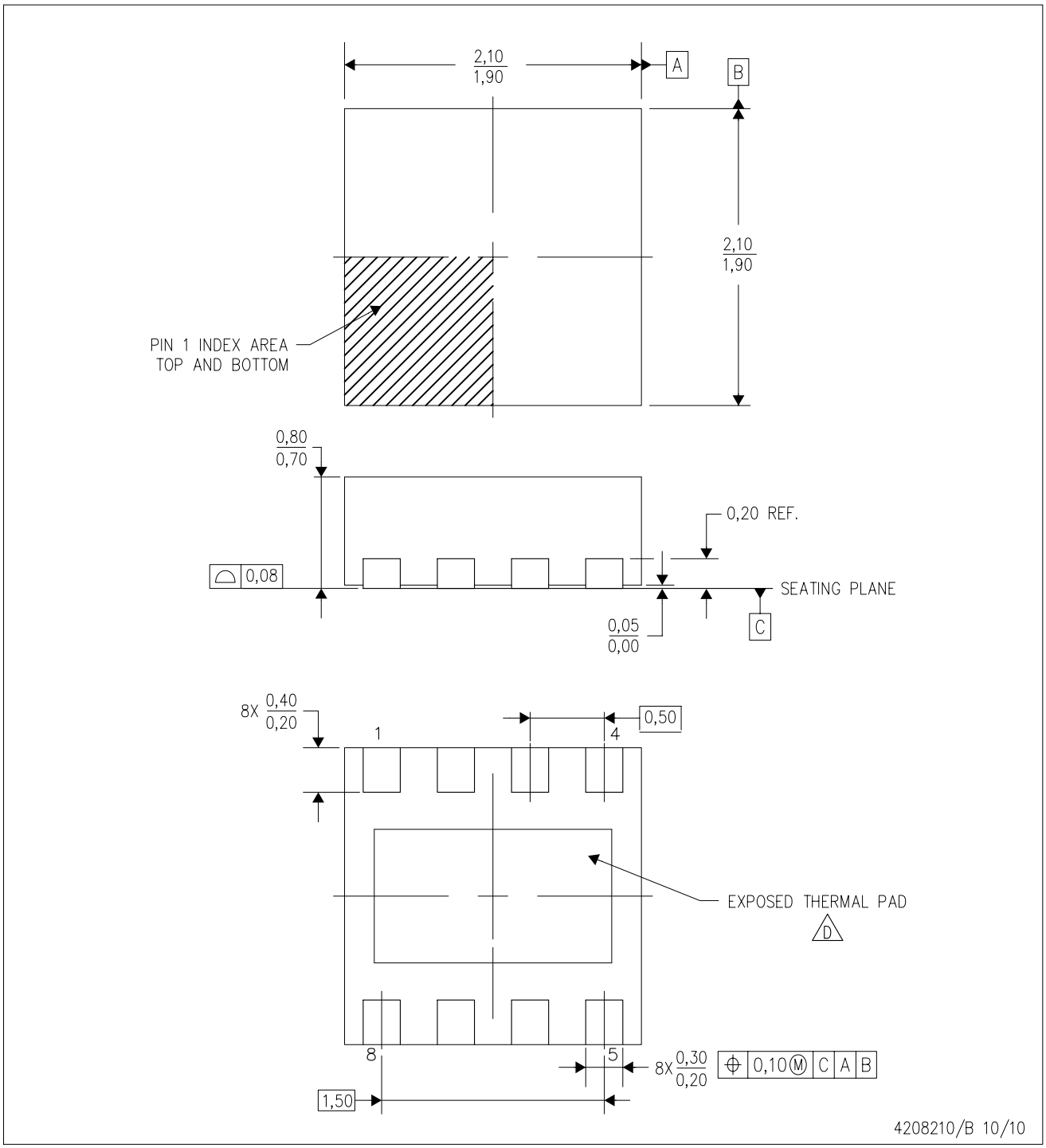
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62065DSGR	WSON	DSG	8	3000	195.0	200.0	45.0
TPS62065DSGR	WSON	DSG	8	3000	205.0	200.0	33.0
TPS62065DSGT	WSON	DSG	8	250	195.0	200.0	45.0
TPS62065DSGT	WSON	DSG	8	250	205.0	200.0	33.0
TPS62067DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62067DSGR	WSON	DSG	8	3000	195.0	200.0	45.0
TPS62067DSGT	WSON	DSG	8	250	195.0	200.0	45.0
TPS62067DSGT	WSON	DSG	8	250	210.0	185.0	35.0

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–229.

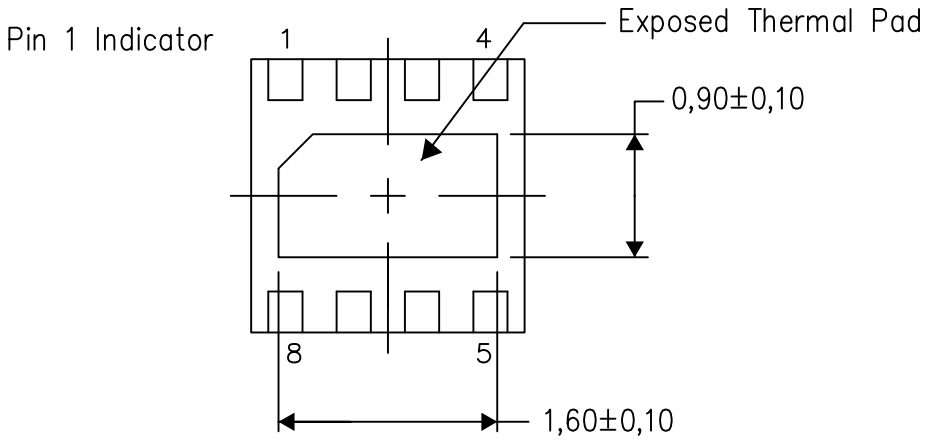
DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



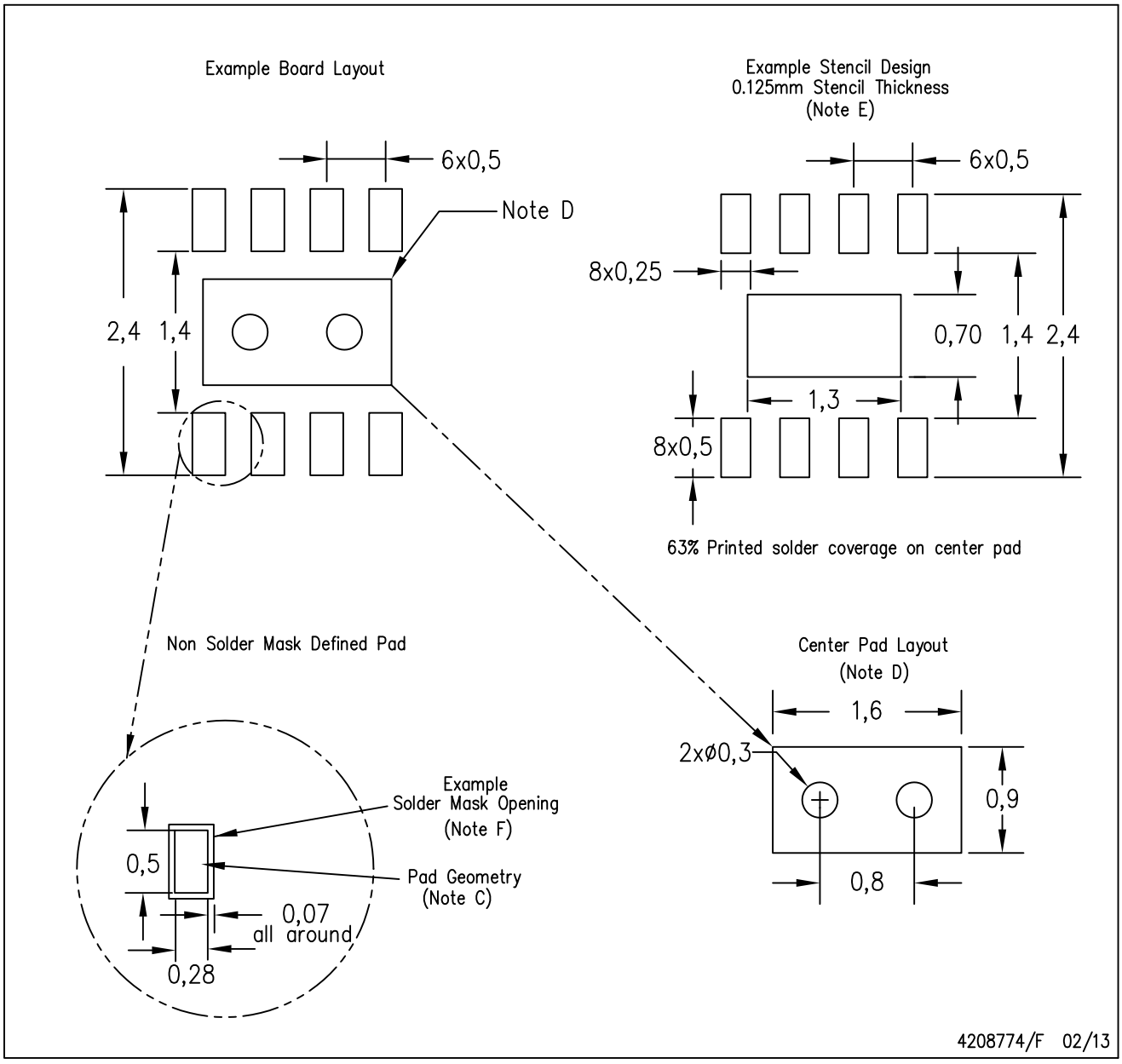
Bottom View

Exposed Thermal Pad Dimensions

4208347/G 08/13

NOTE: All linear dimensions are in millimeters

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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